APPLICATION NOTE

How to Extract ASM-HEMT Model for GaN RF Devices with Thermal Effects Included

KEYSIGHT

PATHWAVE

Introduction

Gallium Nitride (GaN) high electron mobility transistors (HEMTs) are gaining rapid adoption in high-power, high-voltage, and high-frequency applications due to their superior performance such as high saturation velocity, high breakdown voltage, and high sheet carrier density.

However, integrating GaN devices into a circuit design requires accurate and robust circuit simulations. The accuracy of simulations heavily depends on the compact model's ability to predict highly non-linear behavior, including thermal and dynamic memory effects.

The ASM-HEMT model is a physics-based model promoted as an industry-standard model for GaN HEMTs by the Compact Modeling Coalition (CMC). In this document, we will delve into the extraction of the ASM-HEMT core model parameters and temperature scaling. The modeling of trapping effects in GaN HEMTs will be discussed in another application note.

Model description

The ASM-HEMT is a physics-based model. Its formulation consists of three parts:

1. Calculations of surface-potential and channel-charge
2. Terminal current and charge model
3. Various device secondary effects such as trapping and self-healing.

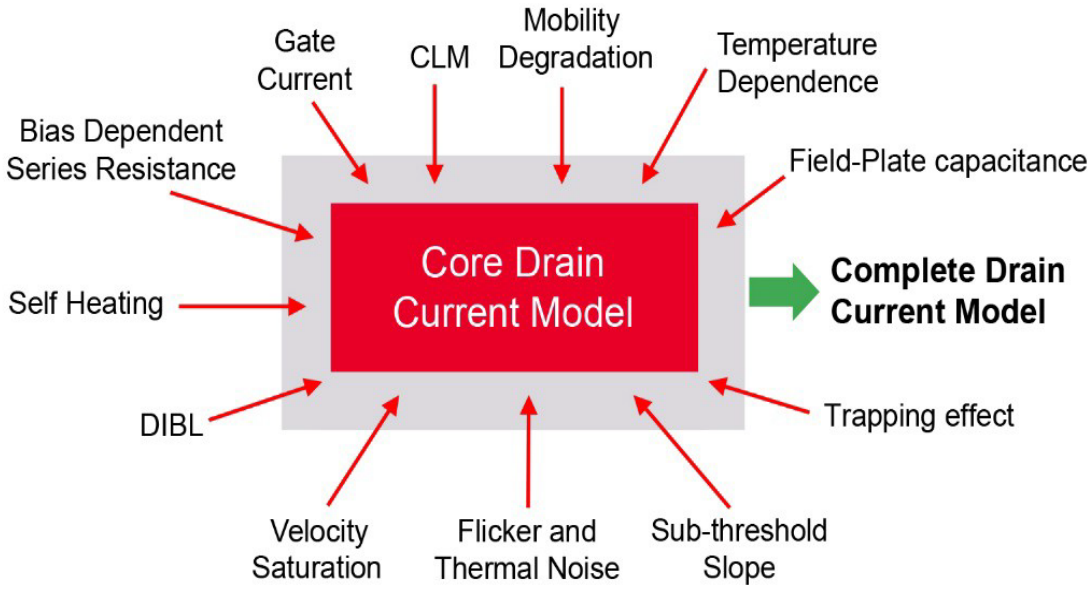


Figure 1. Core surface-potential-based drain current model with various device effects [1].

A physics-based model for 2-DEG describes the core operation of the HEMT device. Analytical solutions are desirable from the compact modeling view because physics-based solutions of the charge and current equations are generally preferable to empirical or measured-based ones since they allow a better insight into the device behavior and enable statistical modeling.

The core model formulations calculate the drain current Id, considering the current continuity and the integration of surface potential along the channel under the gate. Next, various real device effects are added to the core model, including velocity saturation effect, mobility field dependence, subthreshold-slope degradation, non-linear series resistances, channel-length modulation, drain-induced barrier lowering, and self-heating effect temperature dependence.

The accurate models of the capacitances are critical to the transient and frequency response. Therefore, the ASM-HEMT model includes a rigorous charge model.

The parameter extraction described in this document refers to the ASM-HEMT 101.2 example project shipped with PathWave Device Modeling (IC-CAP) 2022 Update 1.0. Each extraction step references the IC-CAP DUT used in the example.

The available ASM-HEMT manual includes the details of the model formulation.

DC / CV parameter extraction

Parameter extraction is an essential step in using a compact model, especially the DC parameter extraction, which is the basis of CV and fT extraction. Various physical effects act on the device simultaneously and interact with each other, and many parameters are involved, complicating the process of parameter extraction. In this paper, we describe a general way of extracting parameters for the ASM-HEMT model.

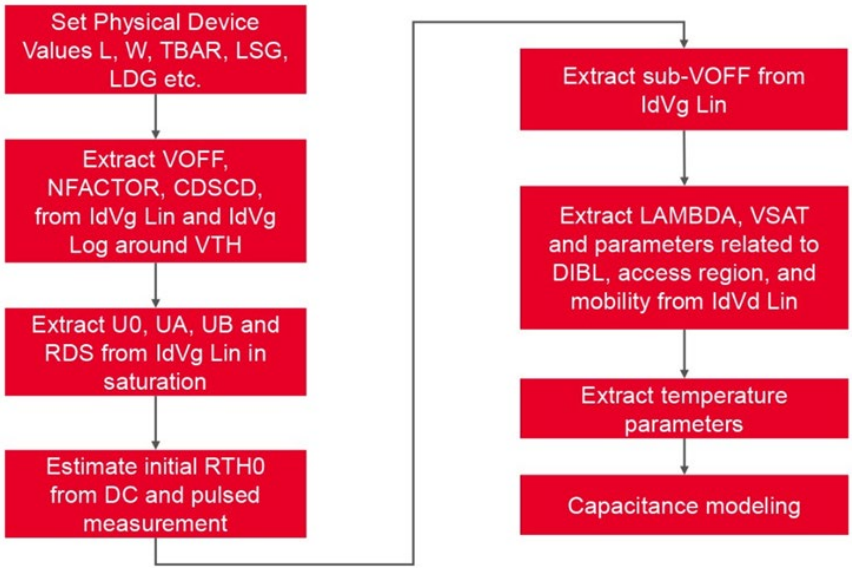


Figure 2. Parameter extraction flow, including intrinsic capacitance and self-heating [1].

The device has eight fingers, its length is 150 nm, and its width is 100 µm. Access regions (AR) measure 1.0 µm and 1.7 µm between the gate-to-source and gate-to-drain, respectively. Figure 2 shows the DC parameter extraction flow.

An example project shipped with PathWave Device Modeling (IC-CAP) implements the strategy outlined in this application note. For convenience, each section below includes a reference to the IC-CAP's DUT used in the example.

Initial settings (DUT: INITIALIZE)

At the beginning of the extraction, we reset the model parameters to default and set the known process and geometry parameters such as device length, width, and number of fingers, and clear any previously simulated data. We also set initial values for temperature, source and drain resistances, parasitic resistances, inductances and capacitances, and RTH0.

Contact resistances (DUT: CONTACT_RESISTANCES)

Next, we characterize DC losses by extracting the contact resistances RTOTALPORT1 and RTOTALPORT2 from measured data at the probe contact.

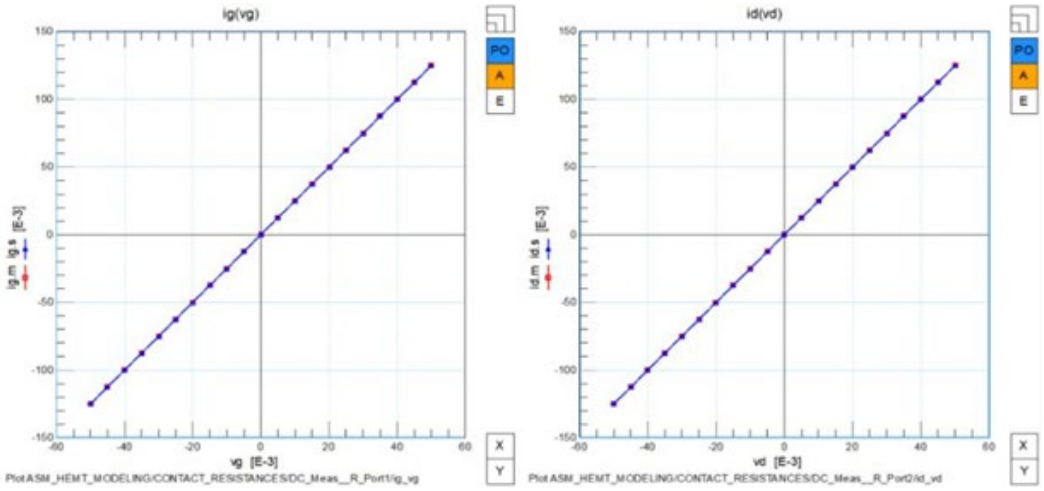


Figure 3. I-V fitting of contact resistances.

DC initial modeling (DUT: DC_MODELING_vt_u0)

By initializing DC parameters, we can extract good starting values of cutoff voltage VOFF, subthreshold slope factor NFACTOR, mobility parameters U0, UA, and UB through the Id-Vg plot in linear scale for multiple Vd. Figure 4 shows the fitting results.

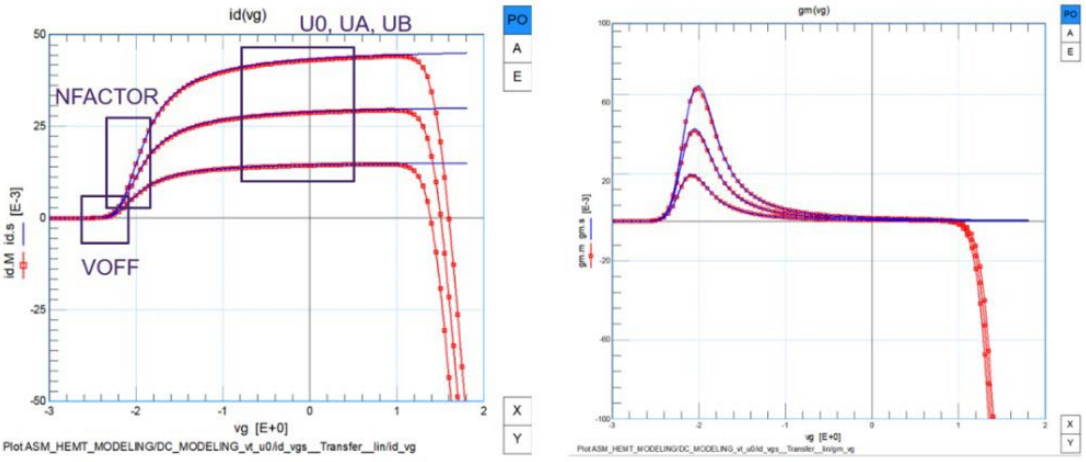


Figure 4. Id-Vg and gm-Vg plots in linear scale for DC initial modeling

CV initial modeling (DUT: CV_Modeling_init)

Similar to DC initialization, we can extract values of multiple parameters of capacitances by fitting the intrinsic gate-source capacitance, CGS, the gate-drain capacitance CGD, and the drain-source capacitance CDS.

In this setup, outer parasitics need to be extracted from measurement and added to the simulated sub-circuit. Figure 5 shows the schematic of the small-signal equivalent circuit. The $C_{GS,P}$, and $C_{GD,P}$, $C_{DS,P}$ parasitic capacitances correspond to Cp11, Cp12, and Cp22 in our example. L_{xg}, L_{xd} and L_{xs} are transmission line inductances representing the connection between the pads and the actual DUT and correspond to LG, LD, and LS in our example. After de-embedding these capacitances and inductances, we can extract the parameters of the CV part from intrinsic plots.

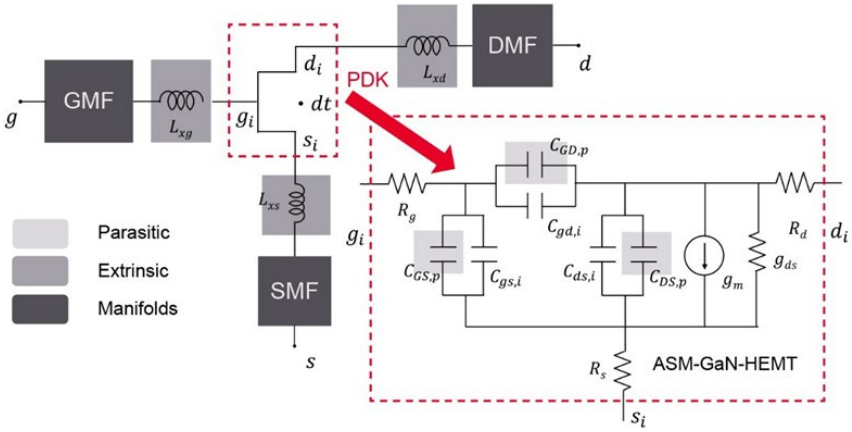


Figure 5. The small-signal equivalent circuit includes intrinsic device and parasitic capacitances and inductances [1].

When fitting intrinsic CV plots, CGSO is optimized to fit CGS at low Vg, CGDO, CGDL, and VDSATCV are optimized to fit CGD at low Vg, CDSO is optimized to fit CDS at low Vd. TBAR, RSC, and RDC are tuned to fit CGS and CGD at Vg close to 0. Figure 6 shows the fitting results.

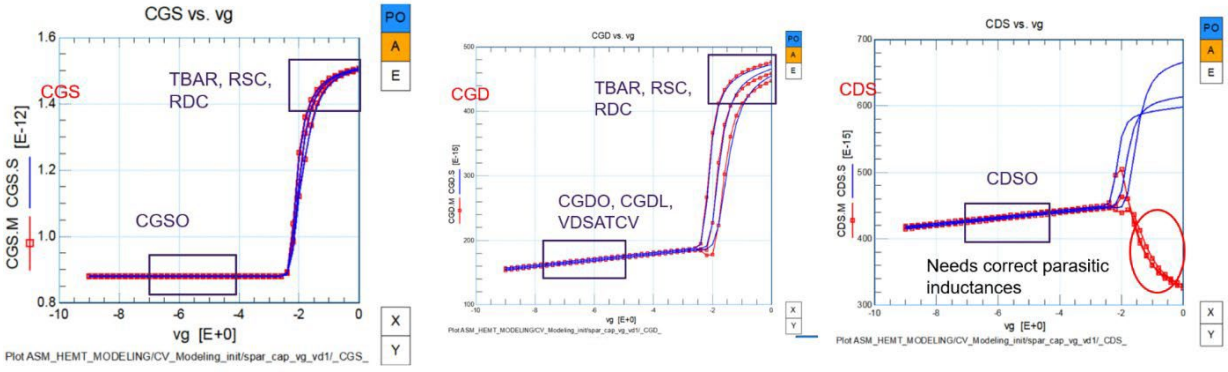


Figure 6. Initial extraction of CV-related parameters by fitting CGS-Vg, CGD-Vg, and CDS-Vg.

Self-heating RTH0 extraction (DUT: DC_RTH_MODELING and DC_PULSED_RTH_MODELING)

In the ASM-HEMT model, the standard R-C thermal network models self-heating. The network contains a thermal resistance RTH0 and a thermal capacitance CTH0. The change in voltage on the thermal node driven by the dissipated power causes a temperature rise in the device, which the simulator considers while solving the circuits.

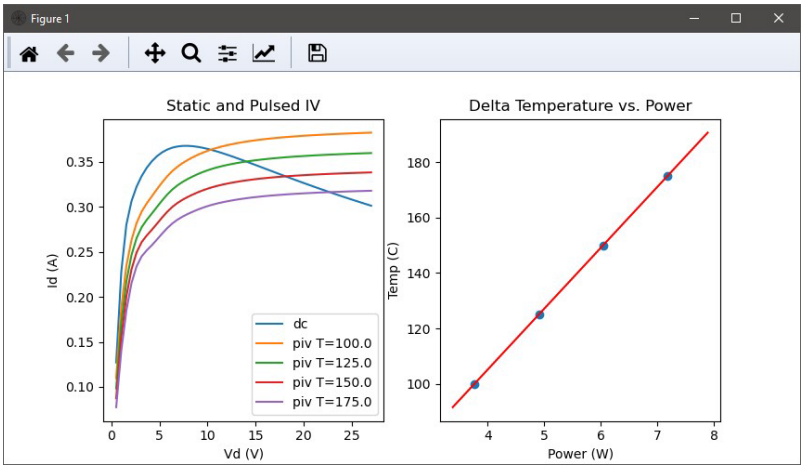


Figure 7. Static Id-Vd at room temperature and pulsed Id-Vd at vd0=vg0=0V to extract RTH0 [2].

To extract RTH0, we deploy two types of data, static Id-Vd at room temperature and pulsed Id-Vd at various temperatures. In pulsed data, the quiescent levels, vd0 and vg0, are equal to 0 V to minimize trapping. Pulses need to be short enough to avoid self-heating. When overlaying static and pulsed characteristics, the curve intersects at points where the current is the same. We can calculate its power value for each intersecting point and plot temperature (in Kelvin) vs. power. The slope of this line is RTH0. The resulting plots are shown in Figure 7. When pulsed data are available, this approach to extract RTH is more intuitive and more straightforward than extracting the RTH0 from the DC static characteristics. In this case, the extracted RTH0 is 22 K/W.

DC modeling (DUT: DC_MODELING and DC_MODELING_TEMP)

After initializing the core parameters, we now improve the parameter extraction of the DC part. In this step, we fit Ig-Vg, Id-Vd, and Id-Vg around VOFF step by step. Then we fit Id-Vd at the low Vd region to avoid the strong self-heating effect. Below is a recommended flow, although changes may be necessary depending on the device.

1. Firstly, we need to set IGSDIO and IGDDIO to relatively large values like 1. We optimize IGSDIO, NJGS, IGDDIO, and NJGD to fit in the log scale around VOFF and above Vg=0 V. The fitting result is shown in Figure 8.

2. Re-tune Id-Vd with VOFF, NFACTOR, U0, UA, and UB if necessary.

3. Optimize ETA0, VDSCALE, CDSCD, and VOFF in linear Id-Vg around VOFF. The fitting result is shown in Figure 9.

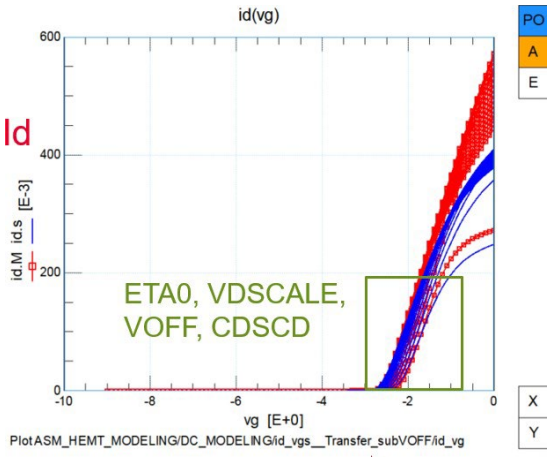


Figure 8. The extraction of Ig-Vg in logarithm scale at Vd=0V.

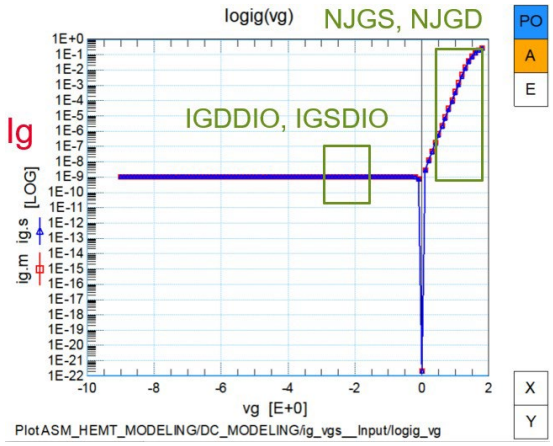
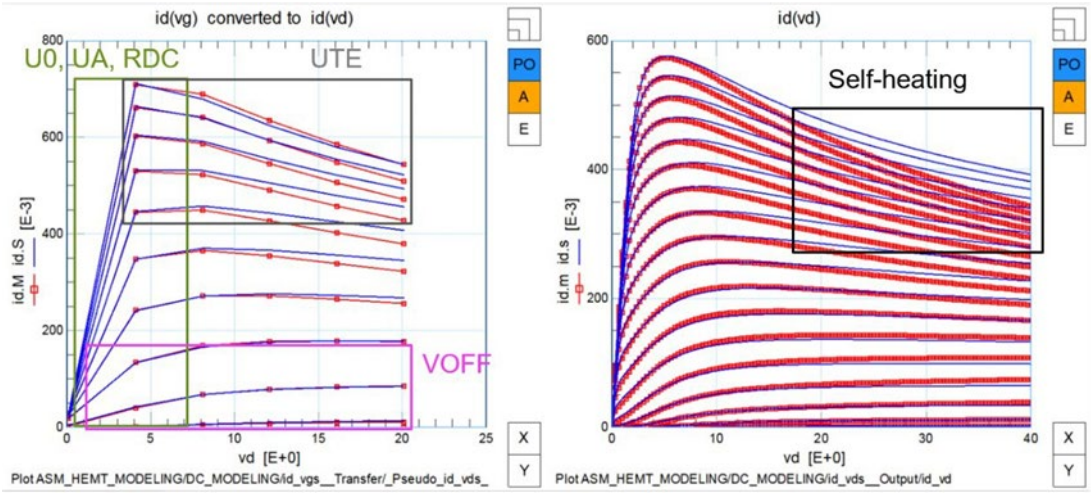


Figure 9. The extraction of Id-Vg in linear scale for multiple Vd around VOFF.

4. Then we fit Id-Vd at the low Vd region to avoid the strong self-heating effect. U0, UA, VOFF, RSC, RDC, and UTE are optimized. The fitting result is shown in Figure 10 (a). Next, we adjust the part affected by self-heating, as shown in Figure 10 (b).



5. KNS0, ATS, UTES, UTED, and RTH0 are optimized. The fitting result is shown in Figure 11.

6. Then, we can make an overall adjustment to Id-Vd with all previously used parameters and those related to the access region, i.e., MEXPACCS, U0ACCS, and U0ACCD. The fitting result is shown in Figure 12.

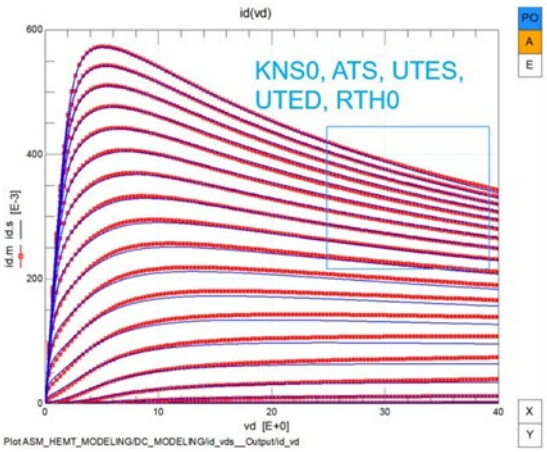


Figure 11. The extraction of Id-Vd at high Vd high Vg with temperature scaling parameters.

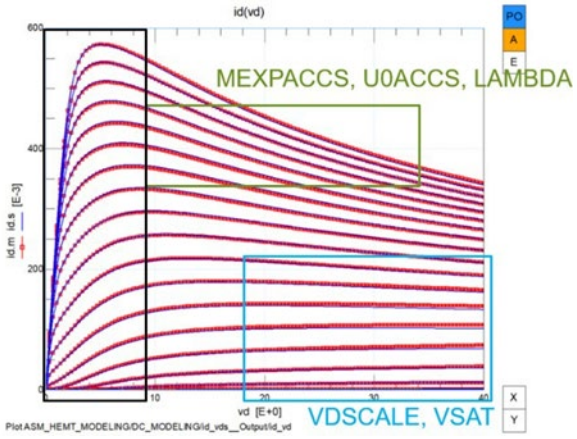


Figure 12. Overall adjustment for Id-Vd.

7. After fitting Id-Vd at room temperature, we also need to check the fitting results of Id-Vd at different temperatures to ensure that our T-scaling parameters are reasonable. The overall fitting results are shown in Figure 13.

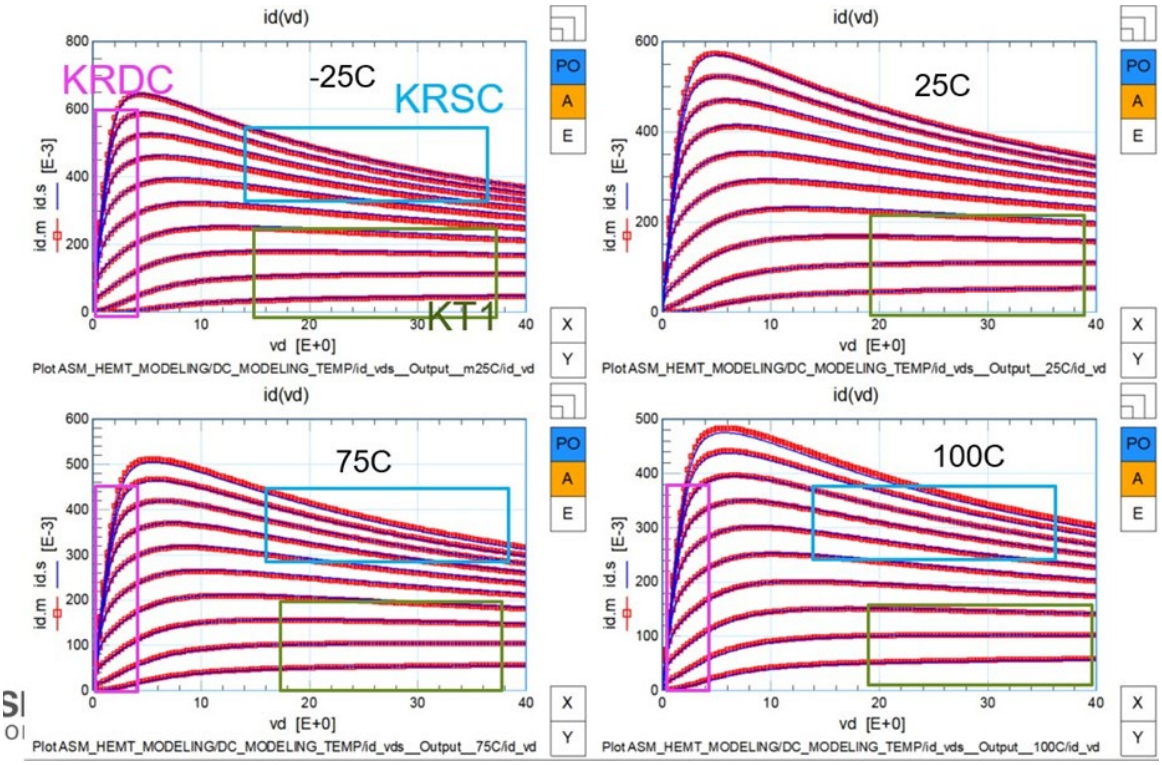


Figure 13. Overall Id-Vd for multiple Vg at different temperatures.

RF parameter extraction

It is essential to accurately extract the RF parameters at various bias points because non-linear behavior is affected. Let's start with CV modeling and then move to S-parameters modeling.

CV modeling (DUT: CV_Modeling)

In the first step, we fit CGS, CGD, and CDS versus Vd at low Vg, Vg = -2.4 V. We select Vg = -2.4 V since it is the expected operating point of the device in a classic Power Amplifier application. CGSO, CGDL, and VDSATCV are tuned to fit CGS-Vd. U0ACCS and UTES can be tuned to change the effective voltage, which is the control voltage for the CV model. Because U0ACCS and UTES also influence Id-Vd in DC_Modeling, we need to check DC and re-tune Id-Vd and CGS simultaneously. CGSO, CGDL, and VDSATCV are tuned to fit CGD-Vd. CDSO, CFD, CJ0, MZ, VBI, AJ, and DJ are tuned to fit CDS-Vd. Note that we need to check these capacitances at the same time.

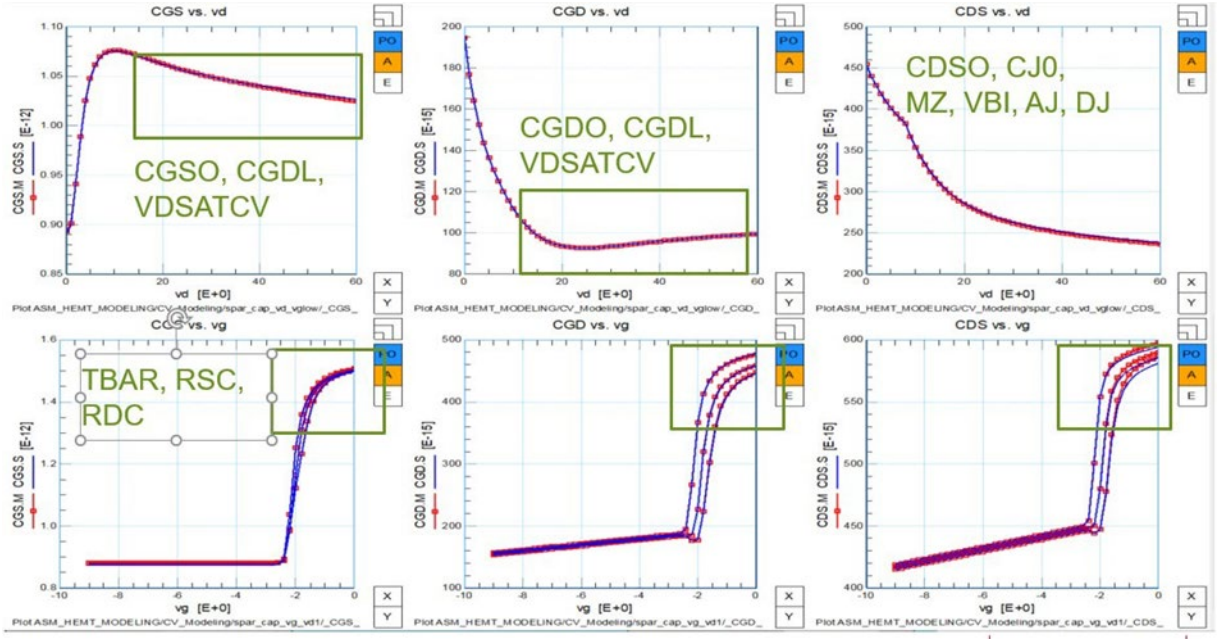


Figure 14. CGS, CGD, and CDS versus Vd (top figures) at Vg = -2.4V. CGS, CGD, and CDS versus Vg (bottom figures) for multiple low Vd.

We are now ready to fit CGS, CGD, and CDS versus Vg at low Vd to avoid self-heating effects with TBAR, RSC, RDC. Fitting results are shown in Figure 14.

So far, we only fit capacitances at low voltage, and they are not influenced by self-heating too much. In the next step, we check the T-dependency of capacitances.

1. Considering self-heating, we fit CGS, CGD, and CDS versus Vd for multiple high Vg. The parameters KTVBI, KTCFG, and KTCFGD, are optimized. In this case, we also tune U0ACCS and ATS a little to better fit CGS. Thus, we need to go back and check Id-Vd in DC_Modeling again.
2. Finally, we fit CGS, CGD, and CDS versus Vg at high Vd. Optimizing the capacitance-related parameters in the previous step and the fitting results are shown in Figure 15.

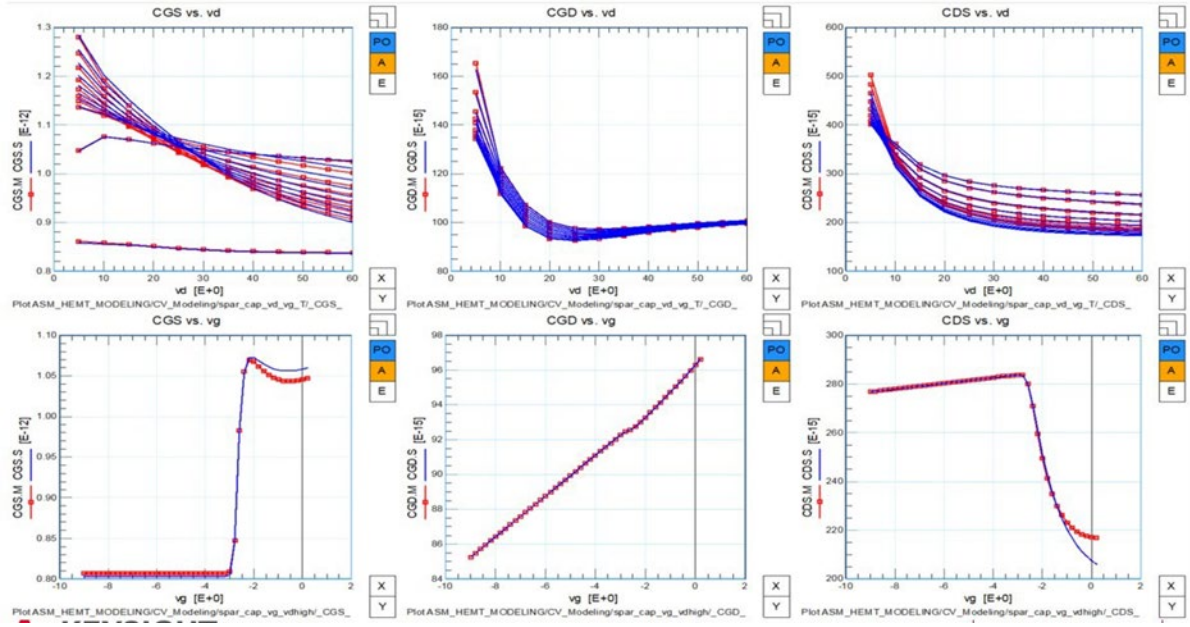


Figure 15. CGS, CGD, and CDS versus Vd (top figures) for multiple Vg. CGS, CGD, and CDS versus Vg (bottom figures) at high Vd.

S-parameters modeling (DUT: SPAR_MODELING)

In this section, we overview S-parameters modeling. If the DC fitting is good enough, S-parameters are mostly influenced by capacitances and bias dependency parameters, which were extracted in CV_Modeling. So, at this point, no new parameters need to be extracted, but we can look at the overall S-parameters under different bias conditions and make a better fitting. Figure 16 shows the fitting results.

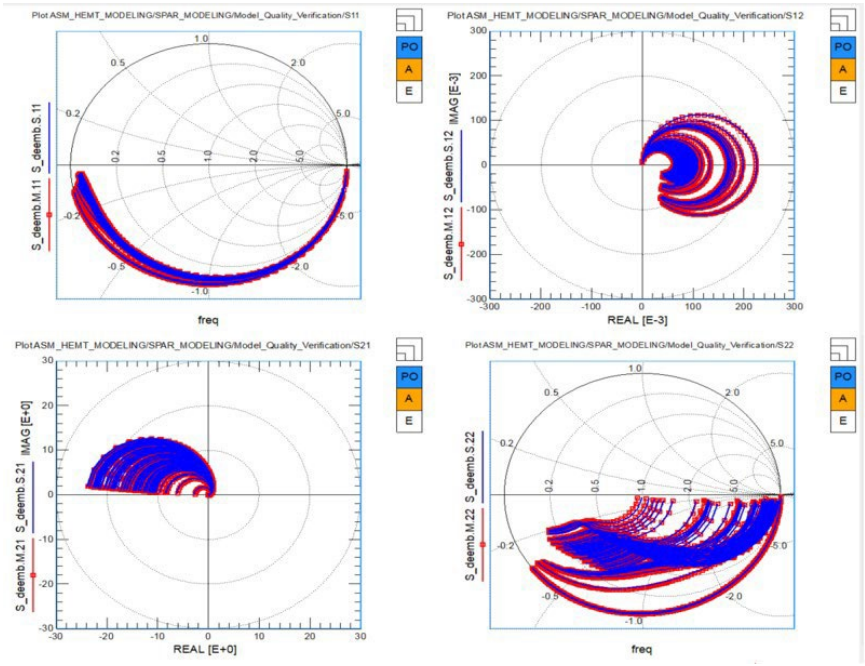


Figure 16. Overall fitting of S-parameters with frequency sweep for multiple Vd and Vg.

Conclusions

This application note outlines a comprehensive strategy to extract and validate the physics-based ASM-HEMT model for GaN HEMTs in RF applications. DC fitting is the most challenging part of the modeling process and is crucial for CV and S-parameters fitting. A comprehensive step-by-step parameter extraction procedure results in a reliable and meaningful model card for RF applications. PathWave Device Modeling (IC-CAP) includes an example project that implements the strategy discussed in this Application Note.

References

[1]. Aamir Ahsan, S. Ghosh, S. Khandelwal, and Y. S. Chauhan, "*Physics-Based Multi-Bias RF Large-Signal GaN HEMT Modeling and Parameter Extraction Flow*," in IEEE Journal of the Electron Devices Society, vol. 5, no. 5, pp. 310-319, Sept. 2017, DOI: 10.1109/JEDS.2017.2724839.

[2]. Makovejev, "Characterization of Thermal *and Coupling Effects in Advanced Silicon MOSFETs,*" Ph.D. dissertation, Sch. of Elect. And Electron. Eng., Newcastle Univ., Newcastle upon Tyne, TWR, 2012