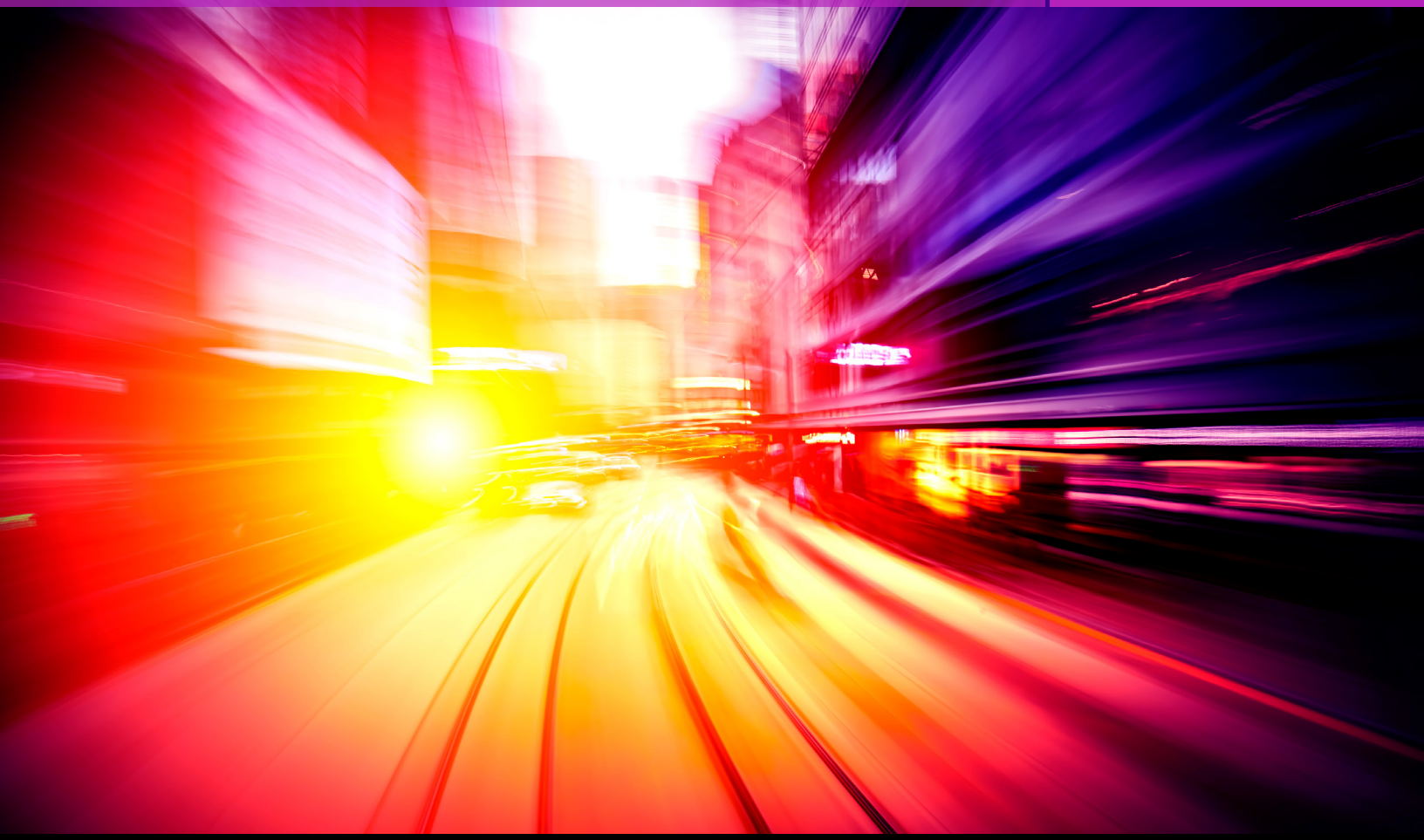
WHITE PAPER



DDR5 - Full Speed Ahead to 400GE

Faster networking speeds require faster memory

KEYSIGHT

Industry adoption of emerging technologies such as 5G and the Internet of Things (IoT) requires data servers and mobile devices to offer faster data rates and performance alongside lower power consumption. Data center operators will transition from 100 gigabit Ethernet (GE) to 400GE to increase network bandwidth for 5G-capable data centers. As data center operators migrate their networks to 400GE, they also need to plan for the next generation of high-speed computing interfaces. Peripheral Component Interconnect Express (PCI Express® or PCIe®) expansion bus will move from PCIe 4.0 to PCIe 5.0, and double date rate (DDR) memory will move from DDR4 to DDR5.

Each new generation of the DDR synchronous dynamic random access memory (SDRAM) standard delivers significant improvements over the previous generation including increased speeds, reduced footprint, and improved power efficiency. However, these improvements introduce new design and test challenges for chip designers and device manufacturers.

The DDR5 standard, defined by the Joint Electronic Devices Engineering Council (JEDEC) organization, will operate at data rates up to 6.0 gigatransfers per second (GT/s) or higher. DDR5 effectively doubles the data rate of DDR4, which supports speeds up to 3.2 GT/s.

Three key highlights in this paper:

- Faster networking speeds require faster memory
- The benefits of DDR5
- DDR5 introduces new design and test challenges

The Benefits of DDR5

With IoT enabling billions of internet-connected devices, data center operators must find ways to meet ever-increasing data and storage demands, while preserving the quality of service and minimizing costs. Power is a premium resource for data center operators and minimizing power consumption is one of their top priorities to reduce operating expenses. Each new generation of DDR SDRAM provides increased data transfer speeds, with more memory in a smaller package size that uses less power. Since power reduction is a critical requirement in mobile devices as well — due to the size and weight constraints of batteries — the JEDEC also introduced a low-power DDR (LPDDR) standard. As the name implies, the LPDDR standard uses lower signal amplitude, reducing power consumption.

DDR timeline

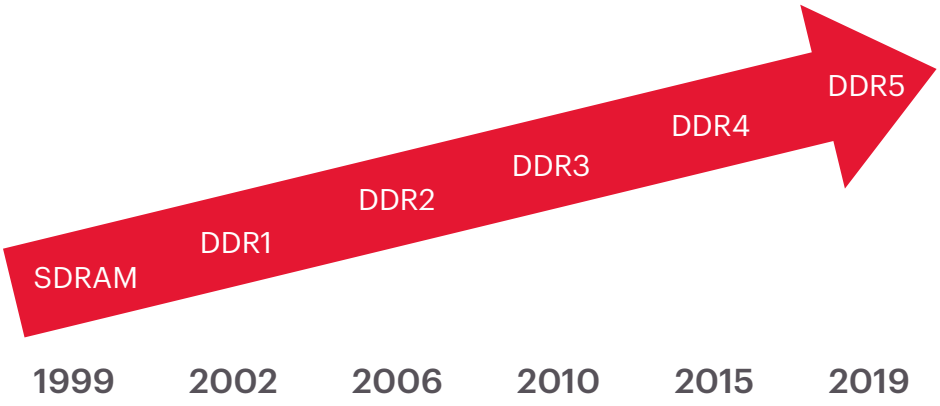


Figure 1. Evolution of the DDR standard

DDR5 will offer improved performance with greater power efficiency as compared to previous generation DRAM technologies. DDR5 will provide double the bandwidth and memory capacity of DDR4, 6 GT/s and one terabit (Tb) of memory respectively, as well as improved power efficiency. DDR5 will provide the performance enhancements and power management needed in the data center to support 400GE networking speeds.

DDR5 Introduces New Design and Test Challenges

As the speed of DDR technology increases, engineers face new design and validation challenges. Design error margins decrease, and signal integrity becomes more challenging to maintain. Test and measurement solutions enable DDR5 designers to optimize their transmitter, receiver, and channel designs for best performance and reliability at the increased data transfer rate of 6 GT/s.

DDR Design and Simulation

Each new version of the DDR standard supports faster access to data stored in memory. Design and simulation of next-generation DDR5 memory designs enable chip designers and device manufacturers to discover issues before silicon tapeout and to maximize the signal integrity of their designs. Using design and simulation tools, DDR5 designers can quickly resolve signal integrity issues, ensure power efficiency, and stay within tight error margins before first prototypes.

DDR Physical Layer Test

DDR5 transmitter (Tx) and receiver (Rx) designs need to comply with the DDR specifications defined by the JEDEC to ensure interoperability with components and devices from other vendors in the system. Each new generation of the standard introduces new DDR physical layer test requirements. DDR5 introduces new receiver compliance tests, not required in previous generations of the standard. Measurement methods and tools developed to test to precise industry specifications allow designers to focus on designing instead of trying to understand the details and requirements of each new generation of the standard. The right test solutions ensure the quality and performance of next-generation DDR designs and help companies get them to market faster.

DDR Protocol Validation

Data corruption is a common symptom encountered during validation of DDR designs, and its root cause can be difficult to determine. Usually, there are either signal integrity or functional issues with the designs. When DDR memory systems do not behave as expected, designers need functional debug, analysis, and protocol compliance validation solutions. Test solutions that provide trace capture and analysis capabilities provide designers the insight required to understand their system's behavior and quickly find the root cause of any issues.

DDR5 design and test solutions ensure:

- Signal integrity at 6 GT/s data transfer speeds
- Compliance to the DDR standard
- Interoperability with components and devices from other vendors

Conclusion

DDR memory is everywhere — not just in servers, workstations, and desktops, but also embedded in consumer electronics, automobiles, and other system designs. The DDR standard provides fast access to data stored in memory in a multitude of consumer devices, as well as in the data center. DDR5, the latest development of the standard, will provide double the bandwidth and memory capacity of DDR4. With data transfer rates up to 6 GT/s and 1 Tb of memory, DDR5 will be able to support 400GE speeds in the data center. Selecting test tools that thoroughly test to DDR5 specifications for design and simulation, characterization, and validation will ensure the performance and interoperability of next-generation DDR5 devices.

For information on how Keysight's solutions can help you address your DDR5 design and test challenges, visit the following web pages:

To accelerate the time-to-market of your gigabit digital designs, check out High-Speed Digital System Design

To learn more about test solutions to simulate, characterize, and validate your DDR designs, check out DDR Design and Test